sidewalls of the metal-containing gate conductor **30** simultaneously when removing the sacrificial spacer **22**.

[0074] In some embodiments of the present invention, a portion of the remaining U-shaped high-k gate dielectric **28** that is not protected by the metal-containing gate conductor **30** which is located abutting the gate corners **31** may be strengthen to reduce the leakage and reliability concerns that may exist at the gate corners **31**. When using a high-k gate dielectric material, increased leakage current and decreased reliability at the gate corners may exist due to stress and/or film deposition. The strengthened region of the remaining U-shaped high-k gate dielectric **28** is labeled as **28'** in FIG. **3**F.

[0075] The strengthening is achieved in the present invention by utilizing a low energy (on the order of about 20 KeV or less) oxygen ion and/or nitrogen ion implantation process. The dose of oxygen and/or nitrogen ions used is typically within a range from about 1E12 to about 1E15 atoms/cm^2, within a dose range from about 1E13 to about 1E14 atoms/cm^2 being more typical. Alternatively, a low temperature oxidation, nitridation or oxynitridation process (temperature on the order of about 950° C. or less) can be used to cause the above mentioned strengthen of the high-k gate material that is present at the gate corners **31**. The net effect of performing one of the above-mentioned techniques is to improve the chemical bonding in the high-k gate dielectric material.

[0076] It is mentioned here that in the present invention the high-k gate dielectric **28** located directly beneath the gate conductor has a height h_3 that is less than the height h_2 of the remaining high-k gate dielectric at the gate corners and that the height h_2 of the remaining high-k gate dielectric at the gate corners is substantially the same or less than the height h_1 of the remaining gate dielectric **18**. In other terms, the gate dielectric has a first height, the high-k gate dielectric that is present at the gate corners has a second height, and the high-k gate dielectric located directly beneath said metal-containing gate conductor has a third height, wherein said first height is substantially the same, or greater than, the second height, and said second height is greater than the third height.

[0077] The remaining drawings show the presence of the strengthened high-k gate dielectric regions **28'** at the gate corners **31**. Although this is illustrated in the remaining drawings, the processing that follows can be used when the optional strengthening step has been omitted.

[0078] FIG. **3**G shows the resultant structure that is formed after forming optional spacer liner **34** and gate spacer **36** within the space that was created when the sacrificial spacer **22** was removed and after substantially all of the high-k gate material located on the vertical sidewalls of the metal-containing gate conductor **20** was removed. The optional spacer liner **34** comprises a first dielectric material which is different from the second dielectric material used in forming the gate spacer **36**. Typically, the spacer liner **34** is comprised of silicon nitride and the gate spacer **36** is comprised of silicon dioxide. In some embodiments, the gate spacer **36** is a low-k (dielectric constant of less than 4.0) dielectric material such as, for example, an organosilicate that includes atoms of at least Si, C, O and H, and the spacer liner **34** comprises silicon oxide.

[0079] The optional spacer liner **34** has a thickness after deposition that is from about 1 to about 10 nm, with about 2 to 5 nm being more typical. The optional spacer liner **34** can be formed by a deposition process such as, for example, atomic layer deposition (ALD), chemical vapor deposition (CVD), low-pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), subatmospheric chemical vapor deposition (SACVD), rapid thermal chemical vapor deposition (RTCVD), high temperature oxide deposition (HTO), low temperature oxide deposition (LTO), limited reaction processing CVD (LRPCVD), spin-on-coating, chemical solution deposition, or any other suitable process. The gate spacer **36** is formed by any suitable deposition process such as CVD and spin-on-coating. It is pointed out herein that a bottom surface of the gate spacer **36** is located atop, or directly on, both the remaining gate dielectric **18** and the high-k gate dielectric that is present at the gate corners **31**. In a conventional prior art structure, the gate spacer is located directly on a surface of the semiconductor substrate.

[0080] In some embodiments of the present invention which is dependant on the geometry of the space in which the gate spacer **36** is to be formed and the deposition process used, a void **38** (see FIG. **2**C) can be present in an interior portion of the gate spacer **36**. The presence of the void has the effect of further reducing the effective dielectric constant of the gate spacer **36** that is employed in the present invention.

[0081] FIG. **3**H illustrates the structure after conductively filled contact vias **40** are formed in the interlevel dielectric material **24** which extend to the surface of the semiconductor substrate **12** that includes the source/drain diffusion regions **14**. The conductively filled contact vias **40** are formed by lithography, etching and filling the contact via thus formed with a conductive material. Optionally, a diffusion barrier such as TiN or TaN can be formed on the exposed sidewalls of the contact via prior to filling the via with the conductive material. The conductive material used in filling the contact openings includes any conductive material including one of the conductive materials used in forming the metal-containing gate conductor **30**.

[0082] In some embodiments of the present invention, the conductively filled contacts vias **40** can be formed into the interlevel dielectric material **24** prior to removing the high-k gate dielectric **28** and the sacrificial spacer **22** from the vertical sidewall of the metal-containing gate conductor **30**.

[0083] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

What is claimed is:

1. A semiconductor structure comprising

at least one metal oxide semiconductor field effect transistor (MOSFET) located on a surface of a semiconductor substrate, said at least one MOSFET comprising a gate stack including, from bottom to top, a high-k gate dielectric and a metal-containing gate conductor, said metal-containing gate conductor having gate corners located at a base segment of the metal-containing gate conductor, wherein said metal-containing gate conductor has vertical sidewalls devoid of said high-k gate dielectric except at said gate corners;

a gate dielectric laterally abutting said high-k gate dielectric present at said gate corners; and